Petent and Trademark Tara: U.S. DEPARTMENT OF COMMERCE Under the Paperwark Reductor Best Applications are Vectored to respond to a collection of inter-REQUEST FOR ACCESS OF ABANDONED APPLICATION UNDER 37 CFR 1.14(a) in re Application of : Harari El.Al. PHULEDSEUBY 337566 4/13/89 JUN 2 5 1998 Group Art Unit Examiner Paper No. **Assistant Commissioner for Patents** Washington, DC 20231 I hereby request access under 37 CFR 1.14(a)(3)(iv) to the application file record of the aboveidentified ABANDONED application, which is: (CHECK ONE) (A) referred to in United States Patent Number 5418752 , column \_\_ (B) referred to in an application that is open to public inspection as set forth in 37 CFR 1.11, i.e., Application No. \_\_\_\_\_\_\_ filed \_\_\_\_\_\_\_ on page \_\_\_\_\_ of paper number\_\_\_\_\_, \_ (C) an application that claims the benefit of the filing date of an application that is open to public inspection, i.e., Application No. \_\_\_\_\_\_\_, filed \_\_\_\_\_\_, or (D) an application in which the applicant has filed an authorization to lay open the complete application to the public. Please direct any correspondence concerning this request to the following address: FOR PTO USE ONLY Approved by: finitials)

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Unit:



# United States Patent [19]

## Harari et al.

[11] Patent Number:

5,418,752

[45] Date of Patent:

May 23, 1995

[54] FLASH EEPROM SYSTEM WITH ERASE SECTOR SELECT

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[21] Appl. No.: 963,851

[22] Filed: Oct. 20, 1992

## Related U.S. Application Data

[62] Division of Ser. No. 337,566, Apr. 13, 1989, abane doned.

[51] Int. Cl.6 ...... G11C 7/00

[58] Field of Search ............ 365/185, 218, 900, 230.03

[56] References Cited

#### U.S. PATENT DOCUMENTS

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R. Wilson, "1-Mbit flash memories seek their role in

system design", Computer Design, Mar. 1, 1989, pp. 30 and 32.

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#### [57] ABSTRACT

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

### 4 Claims, 5 Drawing Sheets

